B1 concl'd

an upper surface having only first and second rows of conductive pads disposed thereon, each of the first and second rows of conductive pads extending along a respective one of the opposite sides of the packaged chips; and

a lower surface having only third and fourth rows of conductive pads disposed thereon, each of the third and fourth rows of conductive pads extending along a respective one of the opposite sides of the packaged chips;

each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the first and second rows disposed on the upper surface of the frame, with each of the leads of one of the packaged chips being electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

B2 9. (Amended) The chip stack of Claim 7 wherein each of the conductive pads of the first and second rows disposed on the upper surface of the frame is electrically connected to a respective one of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.